REMARKS

This is a complete and timely response to the Final Office Action mailed October 23, 2007. Claims 1 and 3-13 are pending in the application. Claim 2 is canceled. Claims 1 and 6-8 are amended. The subject matter of amended claim 1 is supported in at least original claim 2 (canceled), FIG. 3, and the related detailed description. Accordingly, no new matter is added.

In view of the foregoing amendment and following remarks, reconsideration and allowance of the present application and claims are respectfully requested.

Allowable Subject Matter

Applicant gratefully acknowledges the indication in the Office Action that claims 4-13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, first paragraph, set forth in the Office Action and to include all the limitations of the base claim and any intervening claims. However, Applicant believes that claim 1, as amended, is patentable over the cited reference.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1 and 3-13 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Specifically, the statement of the rejection indicates that a single bit (one or more bits) defining an access protocol cannot also define a register access type for each N=2 processors.

Applicant's claim 1, as amended, no longer recites "one or more" bits defining the access protocol. Furthermore, Applicant's originally submitted FIG. 3 and the related detailed description show "bits defining the access protocol." Thus, claim 1, as amended, meets the enablement requirement. Accordingly, Applicant requests that the rejection of claims 1 and 3-13 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,408,671 to Tanaka (hereafter *Tanaka*).

Claim 2 is canceled. Accordingly, the rejection of claim 2 is rendered moot.

A proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen,* 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.,* 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). The test is the same for a process. Anticipation requires identity of the claimed process and a process of the prior art. The claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference. *See, e.g., Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.,* 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). Those elements must either be inherent or disclosed expressly. *See, e.g., Constant v. Advanced Micro-Devices, Inc.,* 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); *Verdegaal Bros., Inc. v. Union Oil Co.,* 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). Those elements must also be arranged as in the claim. *See, e.g., Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); *Carella v. Starlight Archery & Pro Line Co.*, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.,* 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

Accordingly, the single prior art reference must properly disclose, teach or suggest each element of the claimed invention. Applicant's claim 1, as amended, includes at least one feature that is not disclosed, taught or suggested by *Tanaka*.

The Office Action states that:

> As per claim 1, Tanaka teaches a system comprising
> - shared system registers (i.e. the combination of R1 and 21, R2 and 22, R3 and 23, and R4 and 24 in Figs. 1 and 2, each register including one or more bits defining an access protocol (i.e. the four bits one corresponding to each processors, for example, b11-b14 in 21 in Fig. 1), and one

or more bits representing data (i.e. data stored in R1 to R4 in Figs. 1-2); and

- N processors (i.e. processors P1-P4 in Figs. 1-2), N≥ 2, where n is an integer (i.e. n is 4 in Figs. 1-2), each accessing the shared system registers, wherein said one or more bits defining an access protocol include one or more bits that define register access type for each N processors (i.e. bits in 21-24 define access type for each processors P1-P4; see Fig. 2 and Col. 4, lines 20+).

As per claim 3, Tanaka teaches the claimed invention as described above and furthermore, Tanaka teaches that the access type being selected from a group that includes READ, READ/CLEAR, READ/SET, and READ/WRITE, is inherently embedded in the system taught by Tanaka prior art because once the register access is given to any one of the four processors, that processor read or write into that register.

See Office Action pp. 3-4.

Applicant's independent claim 1, as amended, includes "shared system registers, each shared system register including bits defining an access protocol, and one or more bits representing data," and "N processors, N≥ 2, where N is an integer, each of the N processors accessing the shared system registers, wherein said bits defining the access protocol include bits that define a register access type comprising access modes for each of the N processors."

Applicant respectfully submits that both of these features are not expressly or implicitly disclosed by *Tanaka*.

First, *Tanaka* is silent as to the contents of the shared registers R1-R4. Thus, *Tanaka* expressly fails to disclose, teach or suggest a shared system register that includes bits defining an access protocol and one or more data bits.

Tanaka FIG. 1 discloses a shared register control portion 1 situated between processors P1-P4 and shared registers R1-R4. The shared register control portion includes a control means 11, shared bit reset means 12, shared register selector means 13 shared bit set means 14, means for referencing/updating storage area of shared register, access control means 16, shared register directory, as well as shared register storage areas M1-M4. The shared register directory 2, a two-dimensional array of bits that corresponds in a one-to-one relationship with the processors P1-P4 and the shared registers R1-R4 (see *Tanaka*, FIGs. 2-4), does not disclose, teach or suggest

shared system registers including "bits defining an access protocol, and one or more bits representing data."

In marked contrast to Applicant's claimed system, *Tanaka* discloses a one-to-one map or look-up table in the embodiment of a bit array that directs the access control means 16. In accordance with *Tanaka*,

> "The access control means 16 allows access from any processor corresponding to the set bit of each of bit arrays 21 through 24 of the shared register directory to any of the shared registers R1 through R4 corresponding to the bit array including that set bit. Each of the processors P1 through P4 has access to the shared registers R1 through R4 via the access control means 16."

See *Tanaka*, column 3, lines 44-50.

Tanaka does not, inherently or implicitly, disclose, teach, or suggest a shared register that includes bits defining an access protocol and one or more data bits. A bit that indicates when a select processor has access to a shared register denotes connectivity alone and cannot define both an access protocol and include one or more data bits. Applicant's claimed access protocol, as recited in amended claim 1, defines "a register access type comprising access modes for each of the N processors." A register access type comprising an access mode necessarily conveys more information than connectivity.

Consequently, for at least these reasons, *Tanaka* does not disclose, teach or suggest "shared system registers, each shared system register including bits defining an access protocol, and one or more bits representing data," and "N processors, $N \geq 2$, where N is an integer, each of the N processors accessing the shared system registers, wherein said bits defining the access protocol include bits that define a register access type comprising access modes for each of the N processors," as recited in Applicant's independent claim 1. Thus, *Tanaka* does not anticipate the system of amended claim 1. Accordingly, Applicant respectfully submits that claim 1 is allowable and the rejection under 35 U.S.C. § 102(b) should be withdrawn.

Further, Applicant respectfully submits that dependent claim 3 is allowable for at least the reason claim 3 depends directly from allowable independent claim 1. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted).

In addition, Applicant respectfully disagrees with the conclusion that *Tanaka* teaches the access type being selected from the group that includes READ, READ/CLEAR, READ/SET, and READ/WRITE.

In short, the Office Action alleges that once register access is given to any of the four processors that the select processor can read/write into that register. Applicants agree. However, Applicant's claim 3 clearly includes more selections than read and write. As stated above, a bit in a two-dimensional array that indicates access connectivity between a processor and a shared register cannot disclose, teach or suggest a group of access types that includes four members. At most a single bit can denote an on/off or connected/disconnected state. For at least this separate and distinct reason, Applicant's dependent claim 3 is not anticipated by *Tanaka*.

CONCLUSION

For at least the reasons set forth above, Applicant respectfully submits that pending claims 1 and 3-13 are allowable over the cited art of record and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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